Low-Temperature Processing for GaN on GaN Schottky diodes and ohmic contacts

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Vertical GaN-on-GaN devices are considered for next-generation power electronic devices, with improved performance based on the high mobility and high breakdown field of GaN [1]. While lateral AlGaN/GaN HEMTs devices are mature, processing and device concepts for vertical GaN power devices are currently being explored. For example, vertical GaN MOS-devices can have a limited thermal budget after gate oxide deposition. This work will present data on unannealed Schottky diodes and ohmic contact technology.

For Schottky diodes on 5µm-thick-drift layers (ND = 1.9×1016 cm-3) with a basic 500 nm mesa etch, using Ni/Au Schottky contacts, we find a low Ron=2.5 mΩ cm2, reasonable VBR>210V (as limited by measurement tools), a barrier height φb =0.9 eV and a room temperature ideality factor of 1.4, which decreases to 1.05 at 425 K. Surface passivation and effects of low T anneals will further be presented.

For unannealed ohmic contacts on n+ GaN (Nd =1.5×1019 cm-3), we find a low c=1-3×10-6 Ω cm2, demonstrating that unannealed ohmic contacts with good performance are feasible for GaN. Temperature and low T anneal effects will further be presented.

The low-temperature budget process modules will be useful for improved flexibility for vertical GaN device processing.

[1] R. Delgado Carrascon et al., Cryst Growth Des, 22, 7021-7030, (2022).