INVESTIGATION OF ATOMIC LAYER ETCHING FOR FABRICATION OF InP HEMTS

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High electron mobility transistors (HEMTs) based on InGaAs/InAlAs quantum wells are widely-used in microwave low-noise amplifiers. A critical fabrication step is the gate recess etch, presently performed via wet-etching, to place the gate near the channel to maximize transconductance while avoiding gate leakage currents. Wet etching has many limitations, including poor etch-depth control and uniformity. Alternative etch methods which overcome these limitations are thus desirable for realizing high-frequency, low-noise HEMTs.

Here, we report a study of a directional atomic layer etching (ALE) process for InGaAs/InAlAs heterostructures which has potential to satisfy these requirements. The process consisted of an exposure to molecular Cl$_2$ to induce surface modification, followed by a low-energy Ar plasma to sputter the modified surface region while minimally disturbing the underlying film. The stage temperature was varied from \SI{-20}{\celsius} to as low as \SI{-100}{\celsius} to enhance surface chlorination. The etch depth and surface roughness were characterized by atomic force microscopy (AFM).

Figure 1a shows the measured etch per cycle (EPC) versus stage temperature with only Ar ion sputtering and with the full ALE cycle. Negligible sputtering is observed with only Ar ions. With the full cycle, etching is observed at −100 °C. Figure 1b shows an AFM scan of the etched sample, showing increased surface roughness. This result can be attributed to the low volatility of $InCl_x$ etch products. With further process development to remove In species, the ALE processes could be used for the gate recess etch in InGaAs/InAlAs HEMT fabrication, ultimately enabling improved microwave noise performance.