Strain-driven Dislocation Filtering for Epitaxial Growth of InP on (001) Silicon

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Introduction: Heteroepitaxy of InP on CMOS-standard (001) Si substrates offers a promising path for monolithic integration of InP-based optoelectronic devices with silicon photonics components [1-2]. However, the approximate 8% lattice mismatch and consequent high defect density, compounded by anti-phase boundaries (APBs) inherent in growing polar materials on non-polar substrates, significantly degrade the devices' performance and reliability. In this work, we mitigate these issues by introducing an InAsP-based dislocation filter in the InP heteroepitaxy on Si, which effectively reduces the threading dislocation density (TDD) to 7.3×107 cm-2 with a buffer layer of ~2 μm thickness.

Methods: The material growth starts from an APB-free InP/GaAs/Si template originally grown on a 300 mm on-axis (001) Si wafer [3]. This 300 mm InP template was cleaved into smaller pieces for further InP epitaxy within a close-coupled showerhead MOCVD reactor. The InAsP and InP layers were grown at a surface temperature of 590 °C, using TMIn, TBAs, and TBP as group III and group V precursors respectively.

Results and conclusion: We explored the dislocation filtering effects of various strained interlayers. As shown by the electron channelling contrast imaging (ECCI) results, the partially relaxed InAsP-based dislocation filter layer effectively reduces the TDD of 7.5×108 cm-2 to 7.3×107 cm-2. Complementary XRD analysis confirmed the enhanced crystalline quality and the tensile strain in the buffer layers, and correlated these findings with surface morphology as characterized by AFM.