Demonstration of vertical resonant tunneling field-effect transistor using InGaAs/GaAs super lattice nanowires

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Steep-slope transistors, tunnel FETs (TFETs) using tunnel junction have been expected as alternative transistor for ultra-low power integrated circuits because the subthreshold slope is much smaller than the physical limitation of thermionic process. Among the transistors, resonant tunnel FETs (RTFETs) using super lattice (SL) structure have been proposed to enhance on-state current with maintaining steep SS due to resonant tunneling process with ballistic carrier transport [1]. Moreover, the RTFETs have another advantage for novel circuit applications using multi-valued logic technologies [2]. In this report, one-dimensional nano RTFETs, which was composed of selective-area grown n+-InGaAs/InGaAs-GaAs axial SL nanowires (NWs) were demonstrated with vertical gate-all-around (VGAA) architecture. The SL nanowires were grown by selective-area growth. A vertical diode and the VGAA structure using the grown SL nanowires were fabricated by using the same three-dimensional device process flow in previous reports [3]. The demonstrated tunnel junction based on the superlattice exhibited negative-differential resistance (NDR) property with huge current peak-to-valley ratio (PVCR) of 38.8. The VGAA-RTFETs showed large drain current with steep subthreshold slope (SS) of 20 mV/dec under forward bias condition (shown in figure). And the NDR signals were electrically modulated by the gate bias of VGAA structures. Furthermore, very high and sharp transconductance peaks with various supply voltage appeared in the demonstrated VGAA-RTFETs, which implied very fast switching speed. The VGAA-RTFETs would be expected as alternative building-blocks for the ultra-low power consumption integrated circuits and multiple-valued logic architectures.

References:[1] E. Gnani et al., IEEE IEDM Tech. Dig. (2011) 91. [2] M. Andreev et al., Adv. Mat. 34 (2022) 2108830 [3] K. Tomioka et al., Nature 488 (2012) 189.