Template-Assisted Selective Epitaxy of InAs on W metal films

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Introduction

3D integration of III-V semiconductors with Si CMOS is highly attractive since it allows combining new photonic and analog functions with digital processing circuitry. For example, III-V devices such as transistors or photodetectors monolithically integrated on top of Si CMOS circuitry can reduce footprint, minimize latency and allow optimal heat dissipation. Thus far, most 3D integration approaches have used epitaxial growth on Si, layer transfer by wafer bonding or die-to-die packaging.

Methods

We have developed low temperature integration of InAs on W using Si3N4 template assisted selective area metal organic vapor phase epitaxy (MOVPE). Since the W metal can be deposited on any surface, this method allows for III-V integration higher up in the CMOS stack as well as on non-crystalline substrates.

Results

A high yield of single crystalline InAs nanowires for diameters below 75 nm, as observed by transmission electron microscopy (TEM) and electron back scatter diffraction (EBSD), is obtained. For increasing diameter, the yield of single grain nanowires decreases due to multiple nucleation sites on the W in the Si3N4 templates.

Electrical characterization show that the InAs crystals exhibit a low-resistive, ohmic electrical contact to the W film even at cryogenic temperatures. The resistivity increases with template diameter which can be attributed to increased grain boundary scattering. MOSFETs, fabricated from nanowires transferred from the growth substrate, give a field effect mobility of 690 cm2/(V s).

Conclusions

These results demonstrate the feasibility for single-crystalline III-V back-end-of-line integration with a low thermal budget compatible with Si CMOS.